CLAIMS

We claim:

1. A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:

deposition of an electrically conductive bottom electrode layer;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material with a first anneal;

deposition of an electrically conductive top electrode layer; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer.

2. The process of Claim 1, wherein the electrically conductive bottom electrode layer comprises a noble metal.

3. The process of Claim 2, wherein the electrically conductive bottom electrode layer comprises platinum.

4. The process of Claim 1, wherein the ferroelectric dielectric layer comprises PZT.

5. The process of Claim 1 wherein the electrically conductive top electrode layer comprises a noble metal oxide.

6. The process of Claim 5 wherein the electrically conductive top electrode layer comprises Iridium Oxide.

7. The process of Claim 5 wherein the first anneal comprises a rapid thermal anneal at a temperature between five hundred twenty five and six hundred degrees celsius.

8. The process of Claim 7, wherein the first anneal is performed at a temperature of approximately five hundred seventy five degrees celsius for a time between sixty and one hundred twenty seconds.

9. The process of Claim 7 wherein the second anneal is performed at a temperature of between seven hundred and seven hundred fifty degrees celsius.

10. The process of Claim 9, wherein the second anneal is performed at a temperature of approximately seven hundred twenty five degrees celsius for a duration of greater than ten seconds.

11. The process of Claim 10, wherein the second anneal is performed for a duration of approximately twenty seconds.

12. A method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of:

deposition of an electrically conductive bottom electrode layer comprising a noble metal;

deposition of a layer of ferroelectric dielectric material;

annealing the layer of ferroelectric dielectric material with a first anneal;

deposition of an electrically conductive top electrode layer comprising a noble metal oxide; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer.

13. The process of Claim 12, wherein the electrically conductive bottom electrode layer comprises platinum.

14. The process of Claim 12, wherein the ferroelectric dielectric layer comprises PZT.

15. The process of Claim 12 wherein the first anneal is performed in an environment comprising oxygen, the oxygen having partial pressure of less than ten percent of one atmosphere.

16. The process of Claim 15 wherein the first anneal is performed in an environment comprising oxygen at a partial pressure of approximately five percent.

17. The process of Claim 15 wherein the first anneal is performed in an environment comprising a mixture of oxygen and inert gas.

18. The process of Claim 12 wherein the second anneal is performed in an environment comprising a partial pressure of oxygen at a partial pressure of less than five percent of one atmosphere.

19. The process of Claim 18 wherein the second anneal is performed in an environment comprising oxygen at a partial pressure of approximately one percent.

20. The process of Claim 18 wherein the first anneal is performed in an environment comprising a mixture of oxygen and inert gas.

21. The process of Claim 18, further comprising the step of:

depositing an encapsulation layer; and

wherein the second anneal is performed after the step of depositing an encapsulation layer.

22. The process of Claim 21 wherein the second anneal is performed at a temperature of between seven hundred and seven hundred fifty degrees celsius for a time not less than ten seconds.

23. The process of Claim 22 wherein the ferroelectric dielectric layer comprises PZT.

24. The process of Claim 23 wherein the step of depositing the ferroelectric dielectric layer is performed by sputtering.

25. A ferroelectric capacitor comprising:

a adhesion layer comprising titanium dioxide,

a bottom electrode comprising platinum,

a ferroelectric dielectric layer comprising PZT; and

a top electrode layer comprising Iridium Oxide.

26. The ferroelectric capacitor of Claim 25, wherein the ferroelectric dielectric layer comprises grains having a typically columnar structure and has a clear demarcation at an interface between the ferroelectric dielectric layer and the top electrode layer.